Noise and dark performance for FIREBall-2 EMCCD delta-doped CCD detector

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ABSTRACT

The Faint Intergalactic-medium Redshifted Emission Balloon (FIREBall-2) is an experiment designed to observe low density emission from HI, CIV, and OVI in the circum-galactic medium around low-redshift galaxies. To detect this diffuse emission, we use a high-efficiency photon-counting EMCCD as part of FIREBall-2's detector. The flight camera system includes a custom printed circuit board, a mechanical cryo-cooler, zeolite and charcoal getters, and a Nüvü controller, for fast read-out speeds and waveform shaping. Here we report on overall detector system performance, including pressure and temperature stability. We describe dark current and CIC measurements at several temperatures and substrate voltages, with the flight set-up.

Keywords: EMCCD, Photon-counting, Ultraviolet detectors, Dark current, NUVU, CGM, FIREBall

1. INTRODUCTION

FIREBall-2 is a balloon-born ultraviolet (UV) multi-object spectrograph designed to observe faint line emission from the circumgalactic media (CGM) of low redshift galaxies (z $\sim$ 0.7). A previous version of the FIREBall mission has flown twice, in 2006 and 2009.[1,2] Since that time, we have upgraded the spectrograph significantly to increase the field of view, throughput, and number of targets per observation.[3–5] These improvements will yield a factor of 30 increase in overall sensitivity and should provide multiple detections of the CGM in emission for the first time at UV wavelengths. FIREBall-2 will also act as a test-bed for new technologies, including the use of an electron multiplying charge coupled device (EMCCD) processed at JPL to provide UV sensitivity. The delta-doping procedure,[6–8] yields a device with 100% internal quantum efficiency, limited only by surface reflections. Anti-reflection coatings minimize this reflectance and bring the quantum efficiency of the FIREBall-2 device up to > 65% from 200-210 nm.

FIREBall-2 will use a e2v* CCD201-20 in photon counting mode.

1.1 EMCCDs and noise considerations

EMCCDs[9–11] consist of a normal CCD with an extra serial register added after the normal register. This addition to the serial register of an EMCCD contains additional serial register pixels which replace R2 with a DC level pixel and a high voltage (HV) clock. As photo-electrons move through the multiplication register, they undergo impact ionization when passing through the high voltage clock, generating additional electrons. The exact multiplication gain achieved is a stochastic process, which is controlled by the maximum voltage of the HV clock. Each individual transfer has a relatively low probability of multiplication (<2%), but when an electron passes through all 604 multiplication pixels (in the case of an e2v CCD201-20), the final number of electrons generated can be quite large. For our testing, we operate at an electron multiplication (EM) gain of around 1000 e/e.

The advantage of the EM gain process is that it increases the signal from a single photo-electron to a value much larger than the on-chip amplifier read-noise. This process means single events can be detected by a threshold process described more thoroughly in recent works.[12,13] Briefly, pixels with counts greater than 5 times

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the read-noise are considered to have had 1 event. Pixels with counts less than this threshold are considered to have zero events.

Some complications come along with this process. The first is that not all electrons in the device will be amplified above the 5 sigma threshold. The multiplication process is stochastic, so some fraction of real events will not be multiplied enough to be visible. The ratio of the EM gain to the read-noise provides an estimate of the number of events which are not counted because of low amplification, as described by Daigle.[14] Additionally, noise comes from clock induced charge (CIC) and dark current. In a standard CCD, when cooled below -85° C and with normal trapezoidal or square clocks, the noise from dark current will be only a few electrons per hour and CIC will be lower than the added read-noise (assuming a few electrons of read-noise), and thus undetectable. For an EMCCD, both of these noise sources will be amplified in the same manner as photo-electrons.

Dark current can be reduced by operating in inverted mode and by cooling the device further. Recent work exploring dark current vs temperature indicate a lower limit,[15, 16] however most applications operate at -85° C and the behavior below this temperature has not been extensively investigated. Additionally, cold operation of the CCD leads to a significant reduction in charge transfer efficiency (CTE). Keeping these limits in mind, we explore dark current in both an engineering grade and delta-doped EMCCD.

CIC can be reduced by wave shaping and modification of the well depths. Daigle[17] has reported great success in minimizing CIC through the use of sinusoidal and triangular shaped clocks. Both shapes reduced CIC by nearly a factor of 10 at the lowest readout frequencies. Shaped clocks also did not exhibit increased CIC with decreased pixel readout speed.

1.2 Previous detector performance for FIREBall-1

FIREBall-1 used a flight spare of the GALEX[18] near UV (NUV) microchannel plate (MCP).[19] This detector used a Cs_2Te cathode deposited over a thin metal layer on a fused silica window. The NUV detector used for FIREBall-1[1] had a quantum efficiency of around 5 percent in the FIREBall band, somewhat lower than the NUV detector which flew on GALEX. The GALEX MCPs had very low noise, around 193 counts per second over the full detector. This includes both diffuse sources (1.83 counts s^{-1} cm^{-2}) and hotspots (107 counts s^{-1}). Well known effects such as gain sag[20] and other considerations from the MCP were outweighed by its photon counting ability and low noise. Observing techniques such as dithering and limiting the maximum count rate are used in MCP operation to reduce these effects.

For FIREBall-2 a delta-doped EMCCD was selected to replace the MCP in order to increase throughput while maintaining low detector noise. More details about the high QE of the detector can be found in other papers by our group.[4] Our expected QE of ~70% is a significant increase over the GALEX MCP. More recent MCPs since the GALEX flight have achieved higher QE (around 20 percent in the FIREBall band[21]), but a delta-doped AR-coated EMCCD still has an advantage in QE. Our work to minimize detector noise to match that of an MCP is explained below.

1.3 FIREBall-2 detector testing

We describe the ongoing testing of the FIREBall-2 flight detector. This testing includes dark current as a function of both temperature and substrate voltage. We also test clock induced charge as a function of well depth and clock shapes. Finally, most of our testing has been conducted on an engineering grade e2v CCD201-20 procured directly from e2v. We also present initial testing on a delta-doped AR-coated EMCCD processed at JPL and packaged by e2v.

In Section 2 we describe our test set-up. in Section 3 we present the performance of the engineering grade e2v CCD201-20. In Section 3.4.1 we detail initial results from a delta-doped EMCCD. In section 4, we describe our noise performance targets for the FIREBall-2 flight.
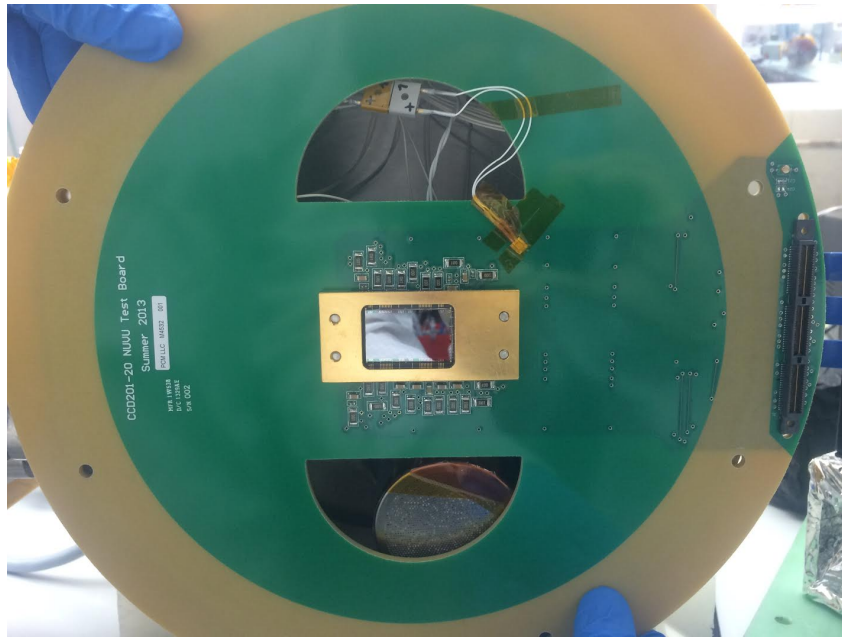
Figure 1. Test PCB holding a delta-doped e2v CCD201-20. The board acts as a rigid harness and vacuum interface board. A gold plated copper clamp supports the EMCCD and connects to the cold finger. The SAMTEC connection can be seen at the right edge of the board. The Nüvü Controller connects here.

2. TEST SET-UP

The FIREBall-2 test set-up is described in more detail in Lingner (expected, 2016).[22] It is briefly summarized here.

The test set-up includes a custom Printed Circuit Board (PCB), which is used as a rigid harness that holds the sensor in place. It also serves as a Vacuum Interface Board (VIB) for the test dewar and incorporates RC filters close to the sensor pins to reduce any noise ripples left in the signal trace. Grounding plates as well as grounding paths are used around the traces to give a low inductance path for the current at high frequencies, to further quiet any noise in the transmission lines. Figure 1 shows a picture of the board with a delta-doped CCD.

Our lab test set-up consists of a Nüvü[†] v.2 CCD Controller for Counting Photons (CCCP),[14] which was chosen for its waveform shaping ability and fast clocking speeds (10 ns resolution). The readout electronics operate at 10 MHz. The Nüvü controller is attached to the PCB with a SAMTEC EQCD high speed coax cable. The EMCCD is supported by a gold plated copper clamp and cooled with a CryoTel MT mechanical cooler (Stirling Engine) from Sunpower[‡]. The EMCCD operating temperature will be between -100 and -120°C with a lift of up to 8 Watts at 24°C ambient temperature and is currently under test in our lab.

Two 10 Watt Omega heaters are used to regulate the temperature; they are attached to the copper clamp just below the EMCCD. Preliminary tests show that the cooler will be operated at a constant input cooling power between 45 to 65 Watts, which corresponds to 70 to 110 Watts battery power and consequently keeps the 60Hz (primary) and 120Hz (secondary) vibrational noise to an acceptable low level. This configuration holds the coldfinger below -165°C, which places the attached 120 mL charcoal getter at a high pumping capacity. Indium is used at all interfaces to minimize any cooling loss. A flexible, multi-layer copper strap conducts the heat from the bottom of the EMCCD via the copper clamp. A Lakeshore 218 controller is used to monitor the temperature across several important surfaces with multiple DT-670 temperature sensors. The detector sits in a vacuum of about 1×10^{-7} Torr. To monitor the pressure inside the dewar, a 354 series Ionization Vacuum Gauge is used. This gauge is turned off during dark current and noise measurements.

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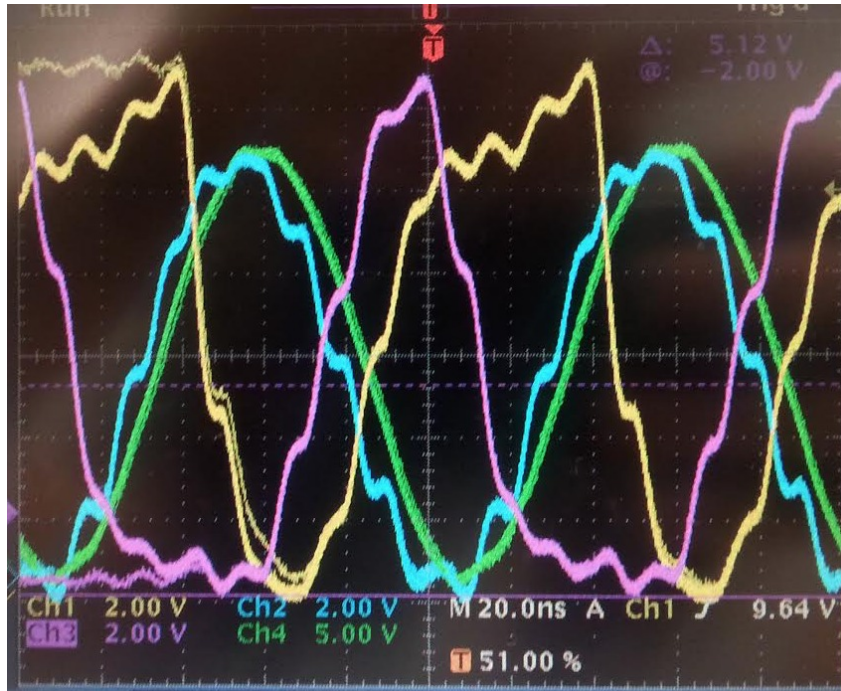
Figure 2. Oscilloscope display of the shaped serial clocks when probed at the PCB pins. R1 is yellow, R2 is blue, R3 is pink, and the High Voltage clock is shown in green (coincident with R2). Clock overlaps are greater than 50% and the High Voltage clock is delayed to overlap with R2 as much as possible.

3. E2V ENGINEERING GRADE CCD201-20 DETECTOR PERFORMANCE

An engineering grade CCD201-20 was procured from e2v for initial testing. This device is a 1k x 1k frame transfer device with an aluminum store shield. Our initial tests used the set-up described above. After verifying device operation and its ability to multiply electrons, we first conducted tests to minimize the amount of CIC in both the parallel and serial registers. With sufficiently low CIC, we explored dark current as a function of temperature and substrate voltage.

3.1 Notes on operation

The initial operation of the engineering grade devices used a clocking scheme based on the e2v data sheet for the CCD201-20.[23] The initial operating conditions used were the nominal values recommended, including -5 to +12 V for the parallel clocks, 0 to +12 V for the serial clocks, and a substrate voltage of +4.5 V. The e2v timing arrangement indicates 50% overlap for parallel and serial clocks. While this overlap worked for the parallel clocks, we found a slightly longer overlap worked best for the serial clocks. The synchronization of the 2nd serial register clock and the high voltage clock is an important component of achieving high gain. In the Nüvü system, this was controlled by a delay time in the resonance system. We found this delay needed to be adjusted for each device we tested. This is likely due to the variance in CCD pin capacitance, which slightly shifts the peak of the resonance system high voltage clock. The other clock times did not need to be changed. Modifications to the system (such as changing the PCB or length of cabling) caused us to make adjustments in both the high voltage delay and the clock overlaps more generally. Figure 2 shows an oscilloscope display of the serial clocks after the optimization described in Section 3.3.2. R1 is yellow, R2 is blue, R3 is pink, and the High Voltage clock is shown in green (coincident with R2).

A standard photon transfer curve was made for each device tested using the multiplication gain readout amplifier. The data sheet read-noise for this amplifier is around 43 e, although "this value is inferred by design and not measured". We found read-noise of 75 e-, with a pre-amp gain of 3 e- ADU^{-1}. This read-noise value is consistant with that measured by Diagle with a CCD201-20 (e-mail correspondence). This read-noise is likely a combination of general system noise and true read-noise from the amplifier. The ratio of read-noise to gain
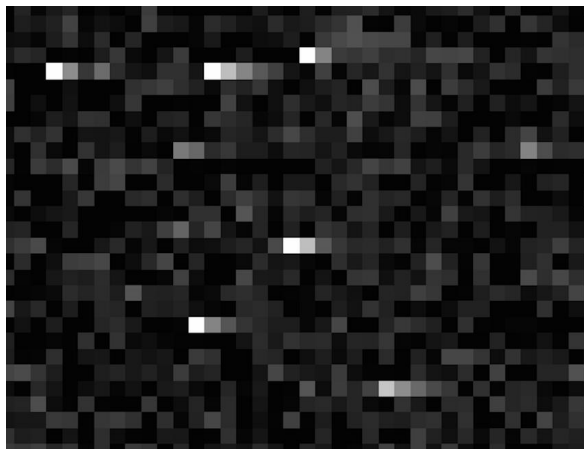
Figure 3. Raw image of a zero second exposure at low temperature (-108° C showing smearing of events. Bright pixels have several trailing pixels with counts significantly above the read-noise.

value is an important value for EMCCD operation, dictating what fraction of events are counted above the 5σ threshold, what number of noise events will be counted, etc. Thus, one future goal in our test set-up is to reduce the system noise to as low a value as possible. CCD designers and users may consider using lower noise amplifiers for future EMCCDs to allow lower gain operation.

3.2 Smearing

As in all CCDs, full well capacity and blooming is a consideration in EMCCDs. As noted in Tulloch,[15] pixels tend to bloom horizontally as the amplification process fills the serial register wells rather than blooming vertically. A further issue is a low temperature smearing process that occurs somewhere in the multiplication register.[17] We observed this phenomenon as low level tails in pixels directly behind pixels with events. This smearing becomes more prominent with both lower temperatures and higher multiplication gains. An example of smeared events is shown in Figure 3. In our image processing, we implement a de-smearing process which uses a statistical analysis of both nearby pixels and the same pixels in images of the same set with equal exposure times. This analysis determines if trailing pixels are above a median plus a threshold within that local region. Pixels that are flagged as smears have their counts de-smeared back into the leading pixel and are given counts with a random Gaussian read-noise level. The exact cause of this smearing is yet to be identified, although Daigle[17] attribute it to general poor CTE. Poor CTE is dependent on temperature, charge packet size, and rate of trap emission, in addition to pixel clocking rate and exact clocking scheme. Further testing, especially of slower pixel clocking speeds, is needed to verify the exact cause and limit this effect.

3.3 CIC

CIC is caused by impact ionization of holes as they move through the Si/SiO2 interface during pixel clocking.[24] The amount of CIC generated depends on the clocking speed (decreasing with increased clocking speed), the substrate voltage (more holes are in the clocks during inversion), clock overlap, and the amplitude of the clock (well depth).

In a normal CCD operation, the single electrons created by clocking are normally masked by read-noise of a few electrons, and so fine tuning of the clocks is usually not necessary. In an EMCCD, electrons generated by clocking, especially in the parallel register or early in the serial register, will be amplified in the same manner as photo-electrons and can be erroneously counted as events. Thus, careful wave-shaping is required to minimize CIC.

CIC in the image area is a combination of both parallel and serial CIC. CIC in over- or pre-scan regions is due only to serial CIC. Serial CIC is measured directly by counting the number of events in the over- and pre-scan regions. Parallel CIC is measured by subtracting the serial CIC value from the total number of events in the image and storage regions.

		Initial Value	Reduced well depth	Shaped & reduced wells
Inverted	Parallel	0.055	0.02	0.001
	Serial	0.02	0.002	0.0007
	Total	0.075	0.022	0.0017
Non-Inverted	Parallel	0.005	0.002	0.001
	Serial	0.05	0.005	0.0005
	Total	0.055	0.007	0.0015

Table 1. Table summarizing CIC measurements for inverted (4.5 V substrate voltage) and non-inverted (0.0 V substrate voltage) operating modes, both before, during, and after optimization.

$$Parallel_{CIC} = Total_{CIC,image} - Serial_{CIC,over-scan} \qquad (1)$$

3.3.1 Parallel CIC

Our work to reduce CIC was conducted in several stages. First, we focused on reducing parallel CIC. Our initial waveform script used trapezoidal or square clocks, with roughly 50% overlap and well voltages from -5 to 7 V. This was close to the clocking scheme specified in the e2v data sheet. Initial parallel CIC levels with this setup were 0.055 events pix^{-1} frame^{-1}, at a substrate voltage of 4.5. In non-inverted mode (substrate voltage of 0.0 V), the parallel CIC was much lower, dropping to 0.005 events pix^{-1} frame^{-1}.

First we experimented with reducing the clock well depths. Our initial high voltage of 7 V is the e2v recommend value. We changed both the overall well depth and the high and low voltage levels. We found that decreasing well depths to an 11 V range provided low CIC while still maintaining good CTE. Well depths below this voltage range caused significant degradation in the CTE. This degradation was most obvious in the central portion of the image area, which developed a hole and upward "orange peel" effect as charge was not effectively transferred through this region. Lower well depths reduced the CIC to 0.01-0.02 events pix^{-1} frame^{-1} at a substrate voltage of 4.5 V. For 0.0 V substrate, lower well depths reduced parallel CIC to 0.002 events pix^{-1} frame^{-1}.

Our second step was to shape the parallel clocks to sine instead of square clocks. This had an immediate effect on CIC, reducing it to 0.001 events pix^{-1} frame^{-1} at a substrate voltage of 4.5 V, while maintaining good CTE. This low CIC was maintained at 0.0 V substrate voltage. Due to these low values, no further wave shaping of the parallel clocks was done.

3.3.2 Serial CIC

We followed the same overall process to reduce the serial CIC. Initially, the serial CIC was 0.02 events pix^{-1} frame^{-1} at 4.5 V substrate, increasing to 0.05 events pix^{-1} frame^{-1} in non-inverted mode. Well depth reduction from 12 V to 10 V lowered serial CIC to 0.002 events pix^{-1} frame^{-1} at 4.5 V substrate. Finally, wave shaping lowered the serial CIC 0.0007 events pix^{-1} frame^{-1} in inverted mode, and to 0.0005 events pix^{-1} frame^{-1} in non-inverted mode. The serial clocks used multi-step shaped clocks.

A combination of wave shaping and well depth optimization reduced total CIC to 0.0017 events pix^{-1} frame^{-1} for inverted mode and 0.0015 events pix^{-1} frame^{-1} for non-inverted mode. Table 3.3.2 summarizes the best results from our CIC optimization process.

3.4 Dark Current

Our work investigated dark current at CCD temperatures between -85 and -125° C. Our set-up has a temperature sensor at the back of the CCD copper clamp, which was typically 3° C below the CCD temperature. Thus, a clamp temperature of -88° C corresponds to a CCD temperature of -85° C. We found a difference in dark current between the image area and the storage area of the frame transfer e2v CCD201-20. The exact reason for this is not clear, but may be related to the differing thickness of the areas or to passivation of the back surface by the aluminium storage shield. We found the storage area had a dark currently roughly half that of the image area.

We measured dark current after optimizing for low CIC as described in Section 3.3. Dark current tests were conducted after a standard turn-on procedure designed to minimize so-called "injected charge" which appeared in
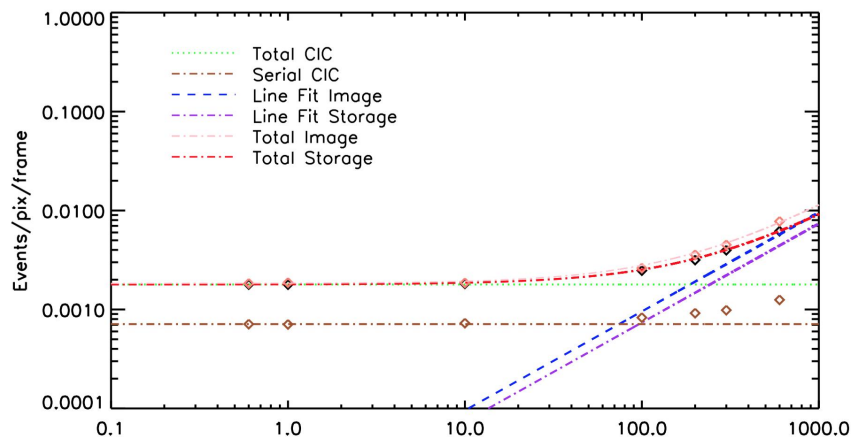
Figure 4. Typical dark current measurement. This example is taken at -108°C. The green and brown lines indicate total and serial CIC, respectively. The blue and purple lines indicate least-squares line fit to the CIC subtracted data. Finally, the pink and red lines indicate the total fit with both CIC and dark current for the image and storage areas of the device. Data points are shown as diamonds. Temperatures refer to the CCD clamp back and thus are 3° C cooler than the CCD surface.

the device as elevated dark current after the controller was reset.[15] The device was turned on at room temperature and allowed to read out for 24 hours. After 24 hours, the device was cooled, while being continuously read out, to -85° C for the first dark current test. Turning the controller off and on while the device was cold caused dark current to increase and then slowly decay at a rate that varied with temperature. To avoid this, we didn't power cycle the controller during dark measurements.

Dark current was measured by taking a set of exposures at increasing exposure times, with five to ten images per exposure time. The high voltage gain was set to 1000 e/e, or as close as possible. The number of events per frame was extracted using a 5 σ threshold and averaged for exposure time. Over-scan and pre-scan regions were also read out for each image. The number of events due to CIC for each set was extracted from the zero second exposure. Additional events with increasing exposure time are attributed to dark current, after cosmic ray removal. For each temperature and substrate voltage configuration, CIC events were subtracted from the total number of events. Then a dark current rate was measured using a least-squares line fit to the remaining counts. The dark current for both the image and storage area was calculated. An example of this measurement is shown in Figure 4.

The dark current measurements we show here are preliminary. As described in Section 3.2, these images were processed using a de-smearing technique to eliminate smeared pixels and reconstruct the un-smeared events. Furthermore, at colder temperatures, cosmic rays become increasingly large sources of noise. The decreased CTE causes cosmic ray events to be smeared out over many pixels. For dark current measurements, these pixels are excised by hand and the rates are corrected to account for the lost pixel numbers.

For the engineering grade e2v CCD201-20, we found dark current decreased with temperature until -105° C. At -85° C, our results agree well with those from Tulloch[15] and Daigle.[16] Below this, there appeared to be a plateau where lower temperature did not significantly reduce dark current. Both image and storage areas had this plateau. Variations in the voltage substrate reduced dark current, as the device is lowered into inversion. Increasing the substrate voltage decreased dark current, while still maintaining the plateau, although the exact value of the plateau did decrease. The plateau may be a combination of a low level light leak plus a non-temperature dependent component that varies with substrate voltage. Further tests are required to determine what contributes to the plateau.

Our results are summarized in Figure 5.

3.4.1 Delta-doped CCD dark current

Initial testing of the performance of a delta-doped device is still ongoing and is not as far along as the engineering grade device testing. Thus we restrict our results to initial dark current measurements at a single voltage substrate
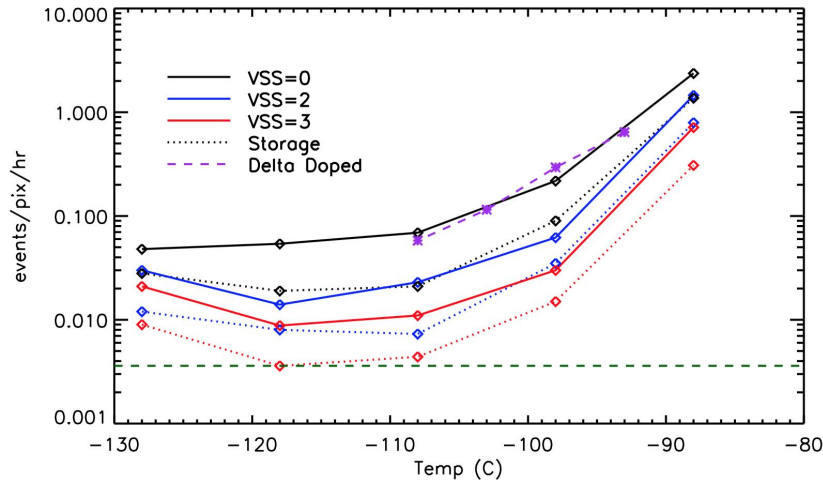
Figure 5. Measured values of dark current vs. temperature. Solid lines indicate dark current for image area while dotted lines indicate dark current for storage area. Colors represent different substrate voltages. Initial dark current measurements of a delta-doped device are shown in purple at a substrate voltage of 0.0 V.

(0.0 V). We find the delta-doped device dark current performance is comparable to that of the engineering grade device dark current. These devices do not have a storage shield and operate in full frame (1k x 2k). Dark current measurements are from the whole device region. Measurements are plotted on Figure 5

4. FIREBALL-2 NOISE GOALS

FIREBall-2's noise requirements are designed for 1000 second exposures. Most uses of EMCCDs operate them at high frame rates with very fast readout speeds. Our operation is in a unique regime in EMCCD spectroscopy in that our primary concern is low dark current for very long exposures. Thus we set a limit of 0.001 events pix^{-1} frame^{-1} for both CIC and dark current, leading to a total of 0.002 events pix^{-1} frame^{-1} in spurious charge. Daigle[14] cites a false positive rate of 1 noise event per million pixels assuming a 5σ cutoff, a flux rate of 0.1 events pix^{-1} frame^{-1}, a gain of around 3000 e/e, with a total noise of 0.001 events pix^{-1} frame^{-1}.

Our total noise during flight operations may be somewhat higher than this, but we expect a low rate of spurious charges per frame. Our future tests include further analysis of delta-doped devices for dark performance and CIC minimization. A version 3 Nüvü controller with digital correlated double sampling and variable pixel clock speeds with 5 ns clock resolution will allow us to reduce noise even further.

FIREBall-2 is expected to fly in 2016.

ACKNOWLEDGMENTS

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